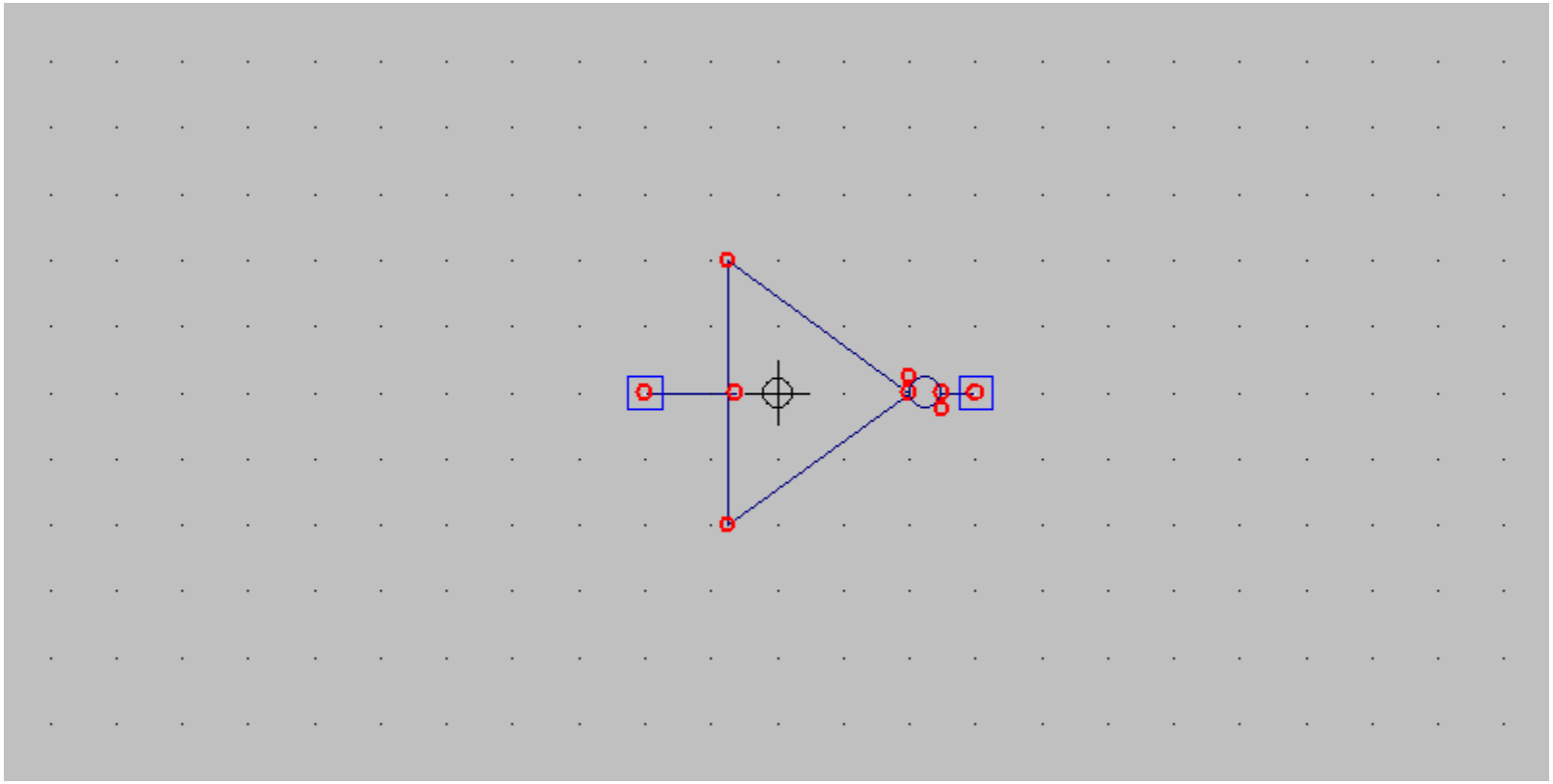
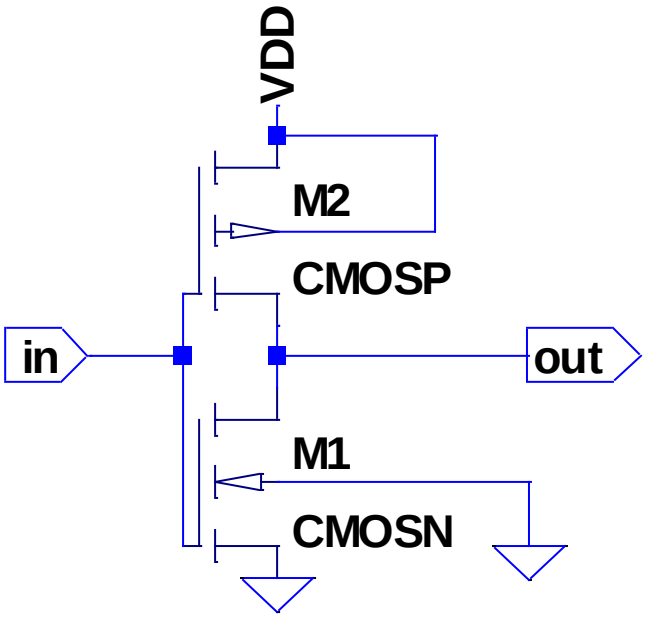
Inverter Symbol



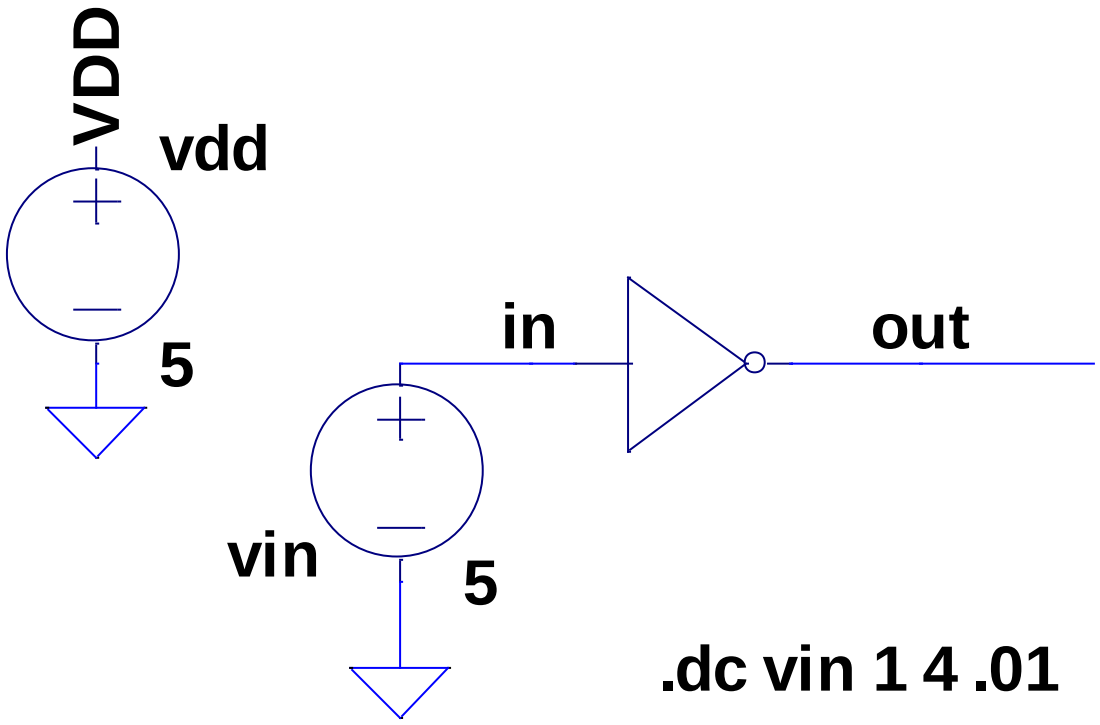
File: inverter.asy

Inverter Circuit




```
.global VDD
.lib ON_C5.lib
```

Test Circuit



Inverter Netlist

```
* C:\ece531\spice4\inverter_test1.asc
XX1 in out inverter
vdd VDD 0 5
vin in 0 5

* block symbol definitions
.subckt inverter in out
M1 out in 0 0 CMOSN l=0.6u w=0.9u
M2 VDD in out VDD CMOSP l=0.6u w=1.5u
.global VDD
.lib ON_C5.lib
.ends inverter

.dc vin 1 4 .01
.backanno
.end
```

Inverter Plot